

UNITED STATES PATENT APPLICATION

OF

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FOR

EMBEDDING RESIN

[0001] The present invention claims the benefit of Japanese Patent Application No. 2001-352511 filed in Japan on December 27, 2000, which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

[0002] The present invention relates to an embedding resin used for embedding, into an opening provided in an insulating substrate, electronic parts such as chip capacitors, chip inductors, and chip resistors, the resin assuming a color having a base color tone selected from among black, blue, green, red, orange, yellow, and violet. More particularly, the present invention relates to an embedding resin suitable for use in, for example, a multi-layer wiring board in which electronic parts are to be embedded, or a package for storing a semiconductor element.

DISCUSSION OF THE RELATED ART

[0003] In recent years, various studies have been performed on multi chip modules (MCMs) in which a number of semiconductor elements are mounted on a build-up wiring board. Typically, electronic parts (such as chip capacitors, chip inductors, and chip resistors) are mounted using solder on the surface of a wiring layer formed on the surface of the wiring board.

[0004] When electronic parts are mounted on the surface of the build-up wiring board, since the parts require predetermined regions for mounting, a limitation is imposed on miniaturization of the wiring board. In addition, when the layout of the wiring for surface mounting is poor, there arises a problem that parasitic inductance of the wiring, which is an undesirable property,

becomes large, resulting in problems in high-frequency operation of an electronic device including the wiring board.

[0005] In order to solve the aforementioned problems, various studies have been performed on the method for embedding electronic parts in an insulating substrate. Japanese Patent Application Laid-Open (*kokai*) No. 11-126978 discloses a method in which electronic parts are mounted by use of solder, in advance, on a wiring board having a transfer sheet formed from metallic foil, and then the parts are transferred. However, the method involves problems in terms of accuracy in the positions of the mounted parts. Japanese Patent Application Laid-Open (*kokai*) No. 2000-124352 discloses a multi-layer wiring board in which an insulating layer is built up on electronic parts embedded in a core substrate.

[0006] In the case where an electronic part is embedded in an insulating substrate such as a core substrate, after a space between the substrate and the electronic part is filled with an embedding resin, and an insulating layer and a wiring layer are built up on the substrate, the electrode of the electronic part must be electrically connected to the wiring formed on the insulating layer, through a metalization technique such as electroless plating.

[0007] The embedding resin is generally colored black in order to prevent random reflection of light, which would otherwise raise problems when a wiring pattern is formed on the built-up insulating layer through exposure and development, or to reduce non-uniformity in color of the resin during curing of the resin. Therefore, carbon or a similar material must be incorporated, as a coloring agent, into the resin.

[0008] However, when a coloring agent having conductivity, such as carbon, is excessively incorporated into the embedding resin, the insulating property of the resin is deteriorated. Therefore, it is important to design the method for coloring the resin black so that random reflection of light is prevented and non-uniformity in color of the resin is reduced during curing of the resin, with the insulating property between electronic parts or between wiring portions formed on the insulating layer being maintained.

SUMMARY OF THE INVENTION

[0009] Accordingly, the present invention is directed to an embedding resin that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

[0010] An object of the present invention is to provide an embedding resin enabling a high mounting density of electronic parts included in a wiring board.

[0011] Another object of the present invention is to provide an embedding resin exhibiting excellent electrical properties, such as insulating property, to prevent random reflection of light and to reduce non-uniformity in color of the resin during curing thereof.

[0012] Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0013] To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, an embedding resin for embedding an electronic part in an insulating substrate assumes a color having a base color tone selected from among black, blue, green, red, orange, yellow, and violet.

[0014] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention. In the drawings:

[0016] Fig. 1 is an explanatory view showing a BGA board formed from a wiring board making use of an embedding resin in accordance with an embodiment of the present invention;

[0017] Figs. 2 through 9 are explanatory views showing an embodiment of the production process of a wiring board making use of an embedding resin of the present invention;

[0018] Fig. 10 is an explanatory view showing a BGA board formed from a wiring board making use of an embedding resin in accordance with an embodiment of the present invention;

[0019] Fig. 11 is an explanatory view showing an embodiment of an FC-PGA-type multi-layer printed wiring board making use of an embedding resin in accordance with the present invention;

[0020] Fig. 12 is a schematic representation of a copper-applied core substrate having a thickness of 400 μm ;

[0021] Fig. 13 is an explanatory view showing the state after the copper-applied core substrate having a thickness of 400 μm has been subjected to patterning;

[0022] Fig. 14 is an explanatory view showing the state after via holes and a through hole have been formed in a substrate including the core substrate and insulating layers formed on both surfaces of the core substrate;

[0023] Fig. 15 is an explanatory view showing the state after the substrate including the core substrate and the insulating layers formed on both surfaces of the core substrate has been subjected to panel plating;

[0024] Fig. 16 is an explanatory view showing the substrate in which the through hole is filled with an embedding resin;

[0025] Fig. 17 is an explanatory view showing the substrate having a through hole formed through punching;

[0026] Fig. 18 is an explanatory view showing the state after a masking tape has been applied onto one surface of the substrate having the through hole formed through punching;

[0027] Fig. 19 is an explanatory view showing the state after laminated chip capacitors have been disposed on a portion of the masking tape, the portion being provided in the through hole;

[0028] Fig. 20 is an explanatory view showing the state after the through hole has been filled with an embedding resin;

[0029] Fig. 21 is an explanatory view showing the state after the surface of the substrate has been planarized through polishing;

[0030] Fig. 22 is an explanatory view showing the state after the polished surface of the substrate has been subjected to panel plating;

[0031] Fig. 23 is an explanatory view showing the state after wiring has been formed through patterning;

[0032] Fig. 24 is an explanatory view showing the state after a build-up layer and a solder resist layer have been formed on the substrate; and

[0033] Fig. 25 is an explanatory view showing an embodiment of a FC-PGA-type multi-layer printed wiring board making use of an embedding resin of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0034] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

[0035] In accordance with the present invention, an embedding resin for embedding an electronic part in an insulating substrate assumes a color tone selected from among black, blue, green, red, orange, yellow and violet. As used herein, the expression "embedding an electronic part" refers to the case where an electronic part is placed in an opening (e.g., a through hole as shown in FIG. 1 or a depression such as a cavity as shown in FIG. 10) provided in an insulating substrate such as a core substrate or in a built-up insulating layer, and then a space formed between the electronic part and the opening is filled with an embedding resin. The opening may

be a through hole formed in a substrate through punching, or a cavity formed by means of multi-layer lamination.

[0036] The substrate used in the present invention is preferably a core substrate, such as FR-4, FR-5, or BT. However, the substrate used in the present invention may be a substrate in which an opening is formed in a core substrate formed by sandwiching a copper foil having a thickness of about 35 μm between sheets of a thermoplastic resin such as PTFE. Alternatively, the substrate used in the present invention may be a substrate in which a build-up layer -- which is formed by laminating an insulating layer and a wiring layer in alternating fashion -- is formed on at least one surface of a core substrate, and an opening portion is formed so as to penetrate at least one of the core substrate and the build-up layer. When this substrate is employed for forming a multi-layer wiring board shown in FIG. 11, the wiring board including capacitors, the thickness of the insulating core substrate formed from a glass-epoxy composite material is advantageously reduced to about 400 μm (i.e., half the thickness of a typical core substrate (800 μm)). Therefore, the height of the wiring board can be reduced. In other example applications, this substrate can be employed for forming a wiring board including electronic parts embedded in a core substrate as shown in FIG. 1 or a wiring board including electronic parts embedded in a build-up layer as shown in FIG. 10.

[0037] Examples of the aforementioned electronic part include passive electronic parts such as chip capacitors, chip inductors, chip resistors, and filters; active electronic parts such as

transistors, semiconductor elements, FETs, and low-noise amplifiers (LNAs); and other electronic parts such as SAW filters, LC filters, antenna switch modules, couplers, and diplexers.

[0038] The embedding resin of the present invention is colored in order to effectively avoid the aforementioned problems in relation to formation of a wiring pattern through exposure and development. Coloring the embedding resin can prevent random reflection of light, which would otherwise raise problems during formation of a wiring pattern on an insulating layer through exposure and development, the insulating layer being built up on the embedding resin; or reduce non-uniformity in color of the resin during curing of the resin.

[0039] The embedding resin is preferably caused to assume any base color selected from among black, blue, green, red, orange, yellow, and violet. When prevention of lowering of resolution due to random reflection of light is an issue of particular importance, the base color of the resin is preferably black, blue, or green, with black being particularly preferred.

[0040] When the embedding resin is colored black, the following substances can be incorporated into the embedding resin: black carbonaceous powder such as carbon black, graphite, or a mixture of carbon black and graphite; powder of a black inorganic oxide such as Cu_2O , CuO , or MnO_2 ; and an azomethine-based black organic pigment such as Chromofine Black A1103.

[0041] Examples of the substance for imparting a blue color to the embedding resin include phthalocyanine-based pigments such as Phthalocyanine Blue and Cyanine Blue 5188; azo pigments such as Variamine Blue; organic pigments including anthraquinone-based pigments such as Anthraquinone Blue; and inorganic oxides such as ultramarine and cobalt blue.

[0042] Examples of the substance for imparting a green color to the embedding resin include phthalocyanine-based pigments such as Phthalocyanine Green and Cyanine Green 5310R; azo pigments such as Chrome Green; organic pigments including triphenylmethane-based pigments such as Malachite Green; and powder of inorganic oxides such as Cr_2O_3 .

[0043] Examples of the substance for imparting a red color to the embedding resin include azo pigments such as Azo Eosine, Azo Naphthol Red, and Lithol Red; organic pigments such as quinacridone, dianthraquinonyl red, and Chromofine Red 6811; and powder of inorganic oxides such as red iron oxide and cadmium red.

[0044] Examples of the substance for imparting an orange color to the embedding resin include azo pigments such as Chrome Orange and 2900 Pelican Fast Orange GR; organic pigments such as benzimidazolone; and inorganic oxides such as molybdate orange.

[0045] Examples of the substance for imparting a yellow color to the embedding resin include azo pigments such as Chrome Yellow, Chromofine Yellow 2080K, and Hansa Yellow; quinoline-based pigments such as Quinoline Yellow; anthraquinone-based pigments such as Anthraquinone Yellow; organic pigments such as benzimidazolone and isoindolinone; and powder of inorganic oxides such as cadmium yellow, chrome yellow, and Titan Yellow.

[0046] Examples of the substance for imparting a violet color to the embedding resin include anthraquinone-based pigments such as Anthraquinone Violet; organic pigments including triphenylmethane-based pigments such as Mitsui Crystal Violet; and powder of inorganic oxides such as manganese violet.

[0047] In order to cause the embedding resin to assume any base color selected from among black, blue, green, red, orange, yellow, and violet, a coloring agent may be used alone.

Alternatively, coloring agents of various colors may be used in combination. In this case, pigments of red, yellow, and blue (i.e., the three primary colors) are preferably used in combination, since the embedding resin can be made to assume any desired color.

[0048] When a coloring agent, other than a conductive coloring agent such as carbon black, is incorporated into the embedding resin, the incorporation amount of the coloring agent is appropriately determined so as to attain a desired color suitable for the production process of a wiring board so that random reflection of light can be prevented or non-uniformity in color of the resin during curing thereof can be reduced. Typically, the incorporation amount of the coloring agent is 0.1-30 mass%.

[0049] Particularly preferably, the embedding resin of the present invention is colored black by incorporating carbon black formed of fine particles into the resin. In order to maintain insulating properties of the embedding resin, carbon black may be incorporated into the resin in an amount of 1.4 mass% or less. When carbon black is incorporated into the embedding resin, insulating reliability and dielectric properties of the resin can be improved, and there can be prevented random reflection of light, which would otherwise raise problems when a wiring pattern is formed through exposure and development on an insulating layer built up on the embedding resin. Further, non-uniformity in color of the resin can be reduced during curing of the resin. Preferably, the amount of carbon black is 1.0 mass% or less. When the incorporation amount of

carbon black exceeds 1.4 mass%, the volume resistance of the embedding resin is greatly lowered, resulting in deterioration of electrical properties.

[0050] In order to effectively solve problems in relation to formation of a wiring pattern through exposure and development, carbon black is incorporated into the embedding resin in an amount of 0.1-1.4 mass%. The amount of carbon black is preferably 0.1-1.0 mass%, more preferably 0.1-0.5 mass%, much more preferably 0.1-0.3 mass%.

[0051] When the incorporation amount of carbon black exceeds 1.5 mass%, the volume resistance of the resin, which is used as an index of insulating property of the resin, becomes less than $1.0 \times 10^{14} \Omega \cdot \text{cm}$.

[0052] The embedding resin of the present invention may contain, as a resin component, at least a thermosetting resin, and at least one inorganic filler. When the embedding resin contains at least a thermosetting resin, the embedding resin can be easily cured through heat treatment after charging of the resin. When an epoxy resin is used as the thermosetting resin, epoxy groups may be directly subjected to cationic polymerization by use of a photo-polymerization initiator such as a dialuriodonium salt.

[0053] In order to perform pre-curing prior to main curing, the thermosetting resin may contain a photosensitive resin. For example, the thermosetting resin may contain a photosensitive resin having an acryloyl group. When an epoxy resin is used as the thermosetting resin, epoxy groups may be directly subjected to photo-polymerization by use of a photo-polymerization initiator, to thereby pre-cure the resin.

[0057] Incorporation of an inorganic filler into the embedding resin is advantageous in that thermal expansion coefficient of the cured embedding resin can be regulated and breakage of the roughed embedding resin is prevented by virtue of the effect of the inorganic filler serving as an aggregate.

[0058] No particular limitation is imposed on the inorganic filler, but crystalline silica, fused silica, alumina, silicon nitride, etc. are preferred. When the inorganic filler is incorporated into the embedding resin, the thermal expansion coefficient of the resin can be effectively reduced. Therefore, reliability of the resin with respect to thermal stress can be improved.

[0059] The particle size of the inorganic filler is preferably 50 μm or less, since a space between electrodes of an electronic part must be easily filled with the embedding resin. When the particle size exceeds 50 μm , a space between electrodes of an electronic part tends to be stuffed with the filler, and the space is insufficiently filled with the embedding resin, so that thermal expansion coefficient of the resin comes to differ greatly from portion to portion. The lower limit of the particle size of the filler is preferably at least 0.1 μm . When the particle size is less than 0.1 μm , fluidity of the embedding resin may fail to be maintained. The particle size of the filler is preferably at least 0.3 μm , more preferably at least 0.5 μm . In order to lower the viscosity of the embedding resin and to fill the space with the resin sufficiently, distribution of the particle size is preferably widened.

[0060] In consideration of high fluidity and filling ability of the embedding resin, preferably, the inorganic filler assumes substantially a spherical shape. Particularly, a silica-based inorganic filler is preferred, since a spherical silica-based inorganic filler is easily available.

[0061] If desired, the inorganic filler may be subjected to surface treatment by use of a coupling agent. This is because, when the inorganic filler is subjected to surface treatment, wettability between the inorganic filler and a resin component is improved, and fluidity of the embedding resin can be improved. Examples of the coupling agent employed include a silane-based coupling agent, a titanate-based coupling agent, and an aluminate-based coupling agent.

[0062] A wiring board in which electronic parts are embedded by use of the embedding resin of the present invention exhibits exposure-development property and insulating reliability. Specifically, flip chip packages including capacitors shown in FIGs. 1 and 10 can be produced by use of the embedding resin. In addition to bump-grid-array-type packages shown in FIGs. 1 and 10, pin-grid-array-type packages can be produced by use of the embedding resin.

[0063] Embodiments of the present invention will now be described in detail.

[0064] A wiring board in which the embedding resin of the present invention is employed, shown in FIG. 1, can be produced through the below-described process. As shown in FIG. 2, a through hole (opening: 2) of predetermined size is formed in a core substrate 1 by use of a die; a backing tape 3 is applied onto a first surface of the core substrate; and the core substrate is placed such that the backing tape is located below the core substrate.

[0065] As shown in FIG. 3, chip capacitors 4 are mounted on predetermined positions of an adhesive surface of the backing tape 3 by use of a chip mounter, the surface being located in the opening 2. In order to embed the chip capacitor in an embedding resin effectively, the chip capacitor preferably has electrodes 5 projecting from the capacitor main body. As shown in FIG.

4, by use of a dispenser, an embedding resin 6 of the present invention is fed into spaces between the opening 2 and the chip capacitors 4 provided in the opening 2.

[0066] The embedding resin 6 is subjected to defoaming and curing at 100°C for 80 minutes, at 120°C for 60 minutes, and at 160°C for 10 minutes. The surface of the cured embedding resin 6 is subjected to rough polishing by use of a belt sander, and then finished through lap polishing.

FIG. 5 shows the surface 60 of the embedding resin 6 after polishing. Subsequently, as shown in FIG. 6, via holes 7 are formed by means of a carbon dioxide gas laser, to thereby expose the electrodes 5 of the chip capacitors 4.

[0067] Thereafter, an exposure surface 61 of the embedding resin 6 is roughed by use of a swelling solution and a KMnO_4 solution. After the roughed surface is activated by use of a Pd catalyst, the surface is subjected to electroless plating and then electroplating, to thereby form a copper plating layer 9. FIG. 7 shows the state after copper plating. A resist (not illustrated) is formed on the plating layer, and a predetermined wiring pattern is formed through patterning. Unwanted copper is removed through etching by use of $\text{Na}_2\text{S}_2\text{O}_8$ /concentrated sulfuric acid.

Subsequently, the resist is removed, to thereby complete formation of wiring 90. FIG. 8 shows the state after formation of the wiring.

[0068] On the wiring, films 14, 15 to serve as insulating layers are laminated, and then cured through heating. Thereafter, the films are irradiated with a laser, to thereby form via holes for connecting the layers. The surface of the outer insulating layer is roughed by use of the aforementioned oxidizing agent, and a predetermined wiring pattern is formed on the insulating layer in a manner similar to that described above. A dry film which is to serve as a solder resist

layer is laminated on the outermost surface of the wiring substrate, and a mounting pattern of a semiconductor element is formed on the dry film through exposure and development, to thereby form a solder resist layer 12. FIG. 9 shows the state after formation of the solder resist layer. Terminal electrodes 13 on which a semiconductor element is to be mounted are subjected to Ni plating and then Au plating. Thereafter, a semiconductor element 18 is mounted on the terminal electrodes through use of a solder reflow furnace. Before the element is mounted, solder balls 17 are formed on the electrodes by use of low-melting-point solder. Spaces between solder balls are filled with an underfill material 21 by use of a dispenser, and the material is cured through heating, to thereby produce the intended wiring substrate shown in FIG. 1.

[0069] The following process may be used to produce a multi-layer wiring board including a substrate in which a build-up layer -- which is formed by laminating an insulating layer and a wiring layer alternately -- is formed on at least one surface of a core substrate, and an opening is formed so as to penetrate the core substrate and the build-up layer (see FIGs. 11 through 25). The production process of a wiring board having an "FC-PGA" structure shown in FIG. 11 will next be described.

[0070] As shown in FIG. 12, a core substrate including an FR-5-made insulating substrate 100 (thickness: 0.4 mm) and copper foil 200 (thickness: 18 μ m) applied on respective surfaces of the insulating substrate is prepared. Properties of the core substrate are as follows: glass transition temperature (Tg) as measured by means of TMA: 175°C; coefficient of thermal expansion (CTE) in a direction parallel to the substrate surface: 16 ppm/°C; coefficient of thermal expansion

(CTE) in a direction perpendicular to the substrate surface: 50 ppm/°C; dielectric constant (ϵ) at 1 MHz: 4.7; and $\tan\delta$ at 1 MHz: 0.018.

[0071] A photoresist film is applied onto the core substrate, and then subjected to exposure and development, to thereby form an opening having a diameter of 600 μm and another opening (not illustrated) corresponding to a predetermined wiring shape. The copper foil exposed to the opening of the photoresist film is removed through etching by use of an etching solution containing sodium sulfite and sulfuric acid. Subsequently, the photoresist film is exfoliated, to thereby obtain a core substrate having an exposure portion 300 shown in FIG. 13 and another exposure portion (not illustrated) corresponding to a predetermined wiring shape.

[0072] The core substrate is subjected to etching by use of a commercially available etching apparatus (CZ treatment apparatus, product of Mec), to thereby rough the surface of the copper foil. Thereafter, an insulating film predominantly containing an epoxy resin (thickness: 35 μm) is applied onto both surfaces of the core substrate. Subsequently, the film is cured at 170°C for 1.5 hours to thereby form an insulating layer 400. Properties of the cured insulating layer are as follows: glass transition temperature (T_g) as measured by means of TMA: 155°C; glass transition temperature (T_g) as measured by means of DMA: 204°C; coefficient of thermal expansion (CTE): 66 ppm/°C; dielectric constant (ϵ) at 1 MHz: 3.7; $\tan\delta$ at 1 MHz: 0.033; percent weight loss at 300°C: 0.1%; percent water absorption: 0.8%; moisture absorption percentage: 1%; Young's modulus: 3 GPa; tensile strength: 63 MPa; and percent expansion: 4.6%.

[0073] As shown in FIG. 14, a via hole 500 for connecting layers is formed in the insulating layer 400 by use of a carbon dioxide gas laser. The via hole assumes a mortar-like shape, and has a top diameter of 120 μm and a bottom diameter of 60 μm . Furthermore, by use of a carbon dioxide gas laser of high power, a through hole 600 (diameter: 300 μm) is formed so as to penetrate the insulating layer 400 and the core substrate. The inner wall surface of the through hole assumes a wavy form (not illustrated) attributed to laser processing. Subsequently, the substrate is soaked in a catalyst activation solution containing palladium chloride, and then the entire surface of the substrate is subjected to electroless copper plating (not illustrated).

[0074] Subsequently, the entire surface of the substrate is subjected to copper panel plating, to thereby form a copper layer 700 (thickness: 18 μm). Through copper plating, a via hole conductor 800 for electrically connecting layers is formed in the via hole 500. In addition, a through hole conductor 900 for electrically connecting the top and bottom surfaces of the substrate is formed in the through hole 600. The resultant substrate is subjected to etching by use of a commercially available etching apparatus (CZ treatment apparatus, product of Mec), to thereby rough the surface of the copper layer. Thereafter, the substrate is subjected to rust preventive treatment (trademark: CZ treatment) making use of a rust preventive agent produced by Mec, to thereby form a hydrophobic surface. The contact angle 2θ of the hydrophobic surface with respect to water as measured through a sessile drop method making use of a contact angle measurement apparatus (product name: CA-A, product of Kyowa Interface Science Co., Ltd.) is 101°.

[0075] Unwoven paper is provided on a pedestal equipped with a vacuum suction apparatus, and the above-treated substrate is placed on the pedestal. A stainless steel mask having a through hole whose position corresponds to the position of the through hole 600 is provided on the substrate. Subsequently, a paste containing a copper filler is placed on the mask, and the through hole 600 is filled with the paste by use of a roller-type squeegee under pressurization.

[0076] As shown in FIG. 15, the paste 1000 in the through hole 600 is pre-cured at 120°C for 20 minutes. Subsequently, as shown in FIG. 16, the surface of the substrate is subjected to polishing (rough polishing) by use of a belt sander, and then subjected to buffing (finishing polishing), to thereby planarize the surface. Subsequently, the paste is cured at 150°C for five hours, to thereby complete the step of embedding the through hole.

[0077] As shown in FIG. 17, a square through hole (opening) 110 (size: 8 mm × 8 mm) is formed by use of a die (not illustrated). Subsequently, as shown in FIG. 18, a masking tape 120 is applied onto the bottom surface of the substrate. Subsequently, as shown in FIG. 19, eight laminated chip capacitors 130 are mounted on a portion of the masking tape 120 by use of a chip mounter, the portion being located in the through hole 110. Each of the laminated chip capacitors includes a laminated body 150 having dimensions of 1.2 mm × 0.6 mm × 0.4 mm and electrodes 140, each electrode having a height 70 μm greater than that of the laminated body.

[0078] As shown in FIG. 20, by use of a dispenser (not illustrated), the through hole 110 in which the laminated chip capacitors 130 are provided is filled with an embedding resin 160 of the present invention. The embedding resin is subjected to defoaming and curing by the

following steps: a primary heating step ($80^{\circ}\text{C} \times$ three hours) and a secondary heating step ($170^{\circ}\text{C} \times$ six hours).

[0079] As shown in FIG. 21, the surface of the cured embedding resin 160 is subjected to rough polishing by use of a belt sander, and then finished through lap polishing. The end surfaces of the electrodes 140 of the chip capacitors 130 are exposed to the polished surface of the embedding resin. Subsequently, the pre-cured embedding resin 160 is cured at 150°C for five hours.

[0080] Thereafter, the polished surface of the embedding resin 160 is roughed by use of a swelling solution and a KMnO_4 solution. After the roughed surface is activated by use of a Pd catalyst, the surface is subjected to electroless plating and then electroplating, to thereby form a copper plating layer 170. As shown in FIG. 22, the plating layer 170 formed on the embedding resin 160 is electrically connected to the end surfaces of the electrodes 140 of the chip capacitors 130. A resist (not illustrated) is formed on the plating layer, and a predetermined wiring pattern is formed through patterning. Unwanted copper is removed through etching by use of $\text{Na}_2\text{S}_2\text{O}_8$ /concentrated sulfuric acid. Subsequently, the resist is removed, to thereby complete formation of wiring as shown in FIG. 23. The surface of the resultant copper wiring is roughed through etching by use of a commercially available etching apparatus (CZ treatment apparatus, product of Mec).

[0081] On the copper wiring, a film 190 to serve as an insulating layer is laminated, and then cured through heating. Thereafter, the film is irradiated with a carbon dioxide gas laser, to thereby form via holes for connecting layers. The surface of the insulating layer is roughed by

use of the aforementioned oxidizing agent, and predetermined wiring 201 is formed on the insulating layer in a manner similar to that described above. A dry film which is to serve as a solder resist layer is laminated on the outermost surface of the wiring substrate, and a mounting pattern of a semiconductor element is formed on the dry film through exposure and development, to thereby form a solder resist layer 210. On the bottom surface of the substrate to which pins for mounting are to be attached, predetermined wiring 230 and a solder resist layer 240 are formed in a manner similar to that described above, to thereby produce a multi-layer printed wiring board shown in FIG. 24 on which the pins are not attached.

[0082] Terminal electrodes 201 on which a semiconductor element is to be mounted are subjected to Ni plating and then Au plating (not illustrated). After a solder paste containing low-melting-point solder is printed on the plated electrodes, solder bumps 220 for mounting a semiconductor element are formed through use of a solder reflow furnace.

[0083] On the surface opposite to the surface on which a semiconductor element is to be mounted, a solder paste containing high-melting-point solder is printed, and then solder bumps 260 for attaching pins are formed through use of a solder reflow furnace. While the wiring board is provided on pins 250 set on a jig (not illustrated), the wiring board is placed in a solder reflow furnace (not illustrated), to thereby attach the pins to the wiring board, thereby producing an FC-PGA-type multi-layer printed wiring board shown in FIG. 25 to which a semiconductor element is not attached. The distance between the position of the tip of each of the pins 250 -- which are attached on the region corresponding to the through hole 110 which has been filled with the

embedding resin 160 -- and the position of the tip as planned is 0.1 mm or less, which is practically acceptable, as measured by use of a projector.

[0084] A semiconductor element 270 is disposed on a position of the surface of the wiring board such that the element can be mounted on the wiring board, and then the wiring board is placed in a solder reflow furnace and heated at a temperature at which only the low-melting-point solder 220 is melted, to thereby mount the semiconductor element 270 on the wiring board.

Subsequently, the mounted portion is filled with an underfill material 300 by use of a dispenser, and then the material is cured through heating, to thereby produce a semiconductor device shown in FIG. 11 including the FC-PGA-type multi-layer printed wiring board on which the semiconductor element 270 is mounted.

[0085] Next, example of embodiments of the present invention will be described in detail.

[0086] An embedding resin was prepared as follows: components were weighed so as to attain a formulation shown in Table 1 and mixed together, and the resultant mixture was kneaded by use of a three-roll mill. Items shown in Table 1 will next be described in detail.

[0087] Epoxy resin

HP-4032D: naphthalene-type epoxy resin of high purity (product of Dainippon Ink and Chemicals, Inc.)

YL-983U: bisphenol-F-type epoxy resin (product of Yuka Shell)

E-850S: bisphenol-A-type epoxy resin (product of Dainippon Ink and Chemicals, Inc.)

N-740: phenol-novolak-type epoxy resin (product of Dainippon Ink and Chemicals, Inc.)

[0088] Curing agent

QH-200: acid anhydride-based curing agent (product of Nippon Zeon Co., Ltd.)

B-570: acid anhydride-based curing agent (product of DIC)

B-650: acid anhydride-based curing agent (product of DIC)

YH-306: acid anhydride-based curing agent (product of Yuka Shell Epoxy K.K.)

YH-300: acid anhydride-based curing agent (product of Yuka Shell Epoxy K.K.)

[0089] Accelerator (curing accelerator)

2MAOK: imidazole-based curing agent (product of Shikoku Corporation)

[0090] Inorganic filler

FB-5LDX: silane-coupled filler (product of Denki Kagaku Kogyo K.K., maximum particle size as measured by means of particle size distribution: 24 μm)

[0091] Coloring agent

(1) Black 1: carbon black #4300 (product of Tokai Carbon Co., Ltd.)

(2) Black 2: Chromofine Black A1103 (product of Dainichiseika Color & Chemicals Mfg. Co., Ltd.)

(3) Blue: Cyanine Blue 5188 (product of Dainichiseika Color & Chemicals Mfg. Co., Ltd.)

(4) Green: Cyanine Green 5310R (product of Dainichiseika Color & Chemicals Mfg. Co., Ltd.)

(5) Red: Chromofine Red 6811 (product of Dainichiseika Color & Chemicals Mfg. Co., Ltd.)

(6) Orange: 2900 Pelican Fast Orange GR (product of Dainichiseika Color & Chemicals Mfg. Co., Ltd.)

(7) Yellow: Chromofine Yellow 2080K (product of Dainichiseika Color & Chemicals Mfg. Co., Ltd.)

[0092] An organic coloring agent was incorporated in an amount of 0.5 mass% (30 mass% only in the case of sample No. 15) into a mixture of epoxy resin, curing agent, and inorganic filler (amount of the mixture: 100 mass%). Carbon black was incorporated, in an amount shown in Table 1, into a mixture of epoxy resin, curing agent, and inorganic filler (amount of the mixture: 100 mass%). "Filler content" is 65 mass%, with the total of the amounts of epoxy resin, curing agent, and filler being taken as 100 mass%. The accelerator content is 0.1 mass%, with the total of the amounts of epoxy resin, curing agent, and filler being taken as 100 mass%. The ratio, on a functional group basis, of the epoxy resin to the curing agent is 100/95. The balance represents the total of the amounts of the epoxy resin and the curing agent. Each of the embedding resin compositions shown in Table 1 was evaluated as follows.

[0093] A sample for evaluation of reliability with regard to volume resistance was prepared as follows. Firstly, through screen printing an embedding resin was printed on a copper plate for Hull cell test so as to attain a width of 60 mm, a length of 90 mm, and a thickness of 100 μ m. Subsequently, the resin was defoamed and cured by the following three heating steps: heating at 100°C for 80 minutes, at 120°C for 60 minutes, and at 160°C for 10 minutes. The resultant sample was subjected to measurement of volume resistance by use of a high resistance meter (model: HP4339B, product of HEWLETT PACKARD). For measurement of volume resistance,

a resistivity cell having a diameter of 26 mm was employed, charging time was set to 20 seconds, and output voltage was set to 100 V.

[0094] A sample for evaluation of yield during exposure and development and for evaluation of volume resistance was prepared as follows. Firstly, the surface of the above-prepared plate sample was roughed by use of a swelling solution and a KMnO_4 solution. The roughed surface was activated by use of a Pd catalyst, and then subjected to electroless plating and electroplating, to thereby form a copper plating layer. A resist was formed on the plating layer, and subjected to exposure and development, to thereby form a comb-shaped wiring pattern having a line width of $40\text{ }\mu\text{m}$ and a line space of $20\text{ }\mu\text{m}$. Unwanted copper was removed through etching by use of $\text{Na}_2\text{S}_2\text{O}_8$ /concentrated sulfuric acid. Thereafter, the resist was exfoliated to thereby complete formation of the wiring. The percentage of the samples which have been passed is referred to as “exposure yield.”

[0095] Criteria for determining whether or not the samples have been passed in the aforementioned evaluations are described below. The evaluation results are shown in Table 2.

Volume resistance: $1.0 \times 10^{14}\text{ }\Omega\cdot\text{cm}$ or more

Exposure yield: 95% or more

[0096] [Table 1]

Sample No.	Epoxy resin	Curing agent	Accelerator	Filler content (%)	Coloring agent content (%)
1	HP-4032D	B-570	2MAOK	FB-5LDX 65	- 0
2	HP-4032D	QH-200	2MAOK	FB-5LDX 65	#4300 0.1
3	HP-4032D	B-570	2MAOK	FB-5LDX 65	#4300 0.3
4	HP-4032D	B-570	2MAOK	FB-5LDX 65	#4300 0.5
5	E-850S	YH-300	2MAOK	FB-5LDX 65	#4300 1.0
6	HP-4032D	B-650	2MAOK	FB-5LDX 65	#4300 1.5
7	E-152	YH-300	2MAOK	FB-5LDX 65	#4300 2.0
8	N-740	B-650	2MAOK	FB-5LDX 65	#4300 2.5
9	HP-4032D	B-570	2MAOK	FB-5LDX 65	A1103 (black 2) 0.5

10	HP-4032D	B-570	2MAOK	FB-5LDX 65	5188 (blue) 0.5
11	HP-4032D	B-570	2MAOK	FB-5LDX 65	5310R (green) 0.5
12	HP-4032D	B-570	2MAOK	FB-5LDX 65	6811 (red) 0.5
13	HP-4032D	B-570	2MAOK	FB-5LDX 65	GR (orange) 0.5
14	HP-4032D	B-570	2MAOK	FB-5LDX 65	2080K (yellow) 0.5
15	HP-4032D	B-570	2MAOK	FB-5LDX 45	5310R (green) 30

[0097] [Table 2]

Sample No.	Volume resistance ($\times 10^{14} \Omega \cdot \text{cm}$)	Exposure yield (%)	Evaluation
1	20.6	94	CC
2	48.0	98	AA
3	35.7	98	AA
4	26.7	97	AA
5	22.7	97	AA
6	17.0	95	BB
7	9.8	96	BB
8	9×10^{-5}	95	DD
9	46.3	98	AA
10	42.7	98	AA
11	36.5	98	AA
12	44.5	97	AA
13	38.8	96	AA
14	32.7	97	AA
15	18.8	98	BB

